IN THE CLAIMS:

Please cancel claims 2 and 3 without prejudice or disclaimer and amend claims 1, 4, 8, and 13-15 as follows:

1. (Currently Amended) An analog-to-digital converter, comprising:

an input for receiving an analog input signal;

a digitizer for producing a digital output signal ~~from a sampled analog input signal~~, said digitizer being switchable, in response to an activation signal, between a power saving mode, in which said digitizer is inactive, and a reconstruction mode, in which said digitizer is operational;

a circuit element for generating said activation signal in response to a trigger event;

a sample-and-hold circuit ~~for~~ having a plurality of storage elements, said sample-and-hold circuit storing ~~a plurality~~ successive groups of ~~successive~~ samples of said analog input signal; ~~and~~

a first set of switch elements connecting said input to said respective storage elements of said sample-and-hold circuit;

a second set of switch elements connecting said respective storage elements of said sample-and-hold circuit to said digitizer; and

a control element for controlling ~~switches to sequentially~~ said first set of switch elements to continually apply ~~said stored samples~~ incoming samples of said analog input signal in a cyclic fashion to said storage elements, said control element further controlling said second set of switch elements when said digitizer is in said reconstruction mode to sequentially apply said samples of said analog input signal stored in said storage elements to said digitizer ~~in response to an activation signal so as to output a digitized version of said input signal as it existed prior to said activation signal~~ with a predetermined delay relative to said incoming samples so as to

permit said digitizer to output a portion of said input signal that arrived at said input prior to the occurrence of said activation signal.

2. Canceled.

3. Canceled.

4. (Currently Amended) An analog-to-digital converter as claimed in claim ~~3~~ 1, wherein said ~~sampling circuits~~ storage elements each comprise a capacitor.

5. (Original) An analog-to-digital converter as claimed in claim 4, comprising eight said capacitors.

6. (Original) An analog-to-digital converter as claimed in claim 1, further comprising a comparator for generating said activation signal in response to said input signal reaching a threshold level.

7. (Original) An analog-to-digital converter as claimed in claim 1, wherein said control element is a state machine.

8. (Currently Amended) A method of converting an analog signal to a digital signal, comprising:

feeding successive samples of said analog signal to a sample-and-hold circuit;

storing groups of successive samples of said input signal in said sample-and-hold circuit; ~~and~~

providing a digitizer for producing a digital output signal, said digitizer being switchable, in response to an activation signal, between a power saving mode, in which said digitizer is inactive, and a reconstruction mode, in which said digitizer is operational;

generating said activation signal to switch said digitizer into said reconstruction mode in response to a trigger event; and

after generating said activation signal, sequentially applying said stored samples with a delay of at least one sample period relative to incoming samples to a said digitizer ~~in response to an activation signal, said digitizer producing a digital output signal representing said input signal as it existed prior to said activation signal~~ so as to permit said digitizer to output a portion of said input signal that arrived at said input prior to the occurrence of said activation signal.

9. (Original) A method as claimed in claim 8, wherein said samples are stored in a series of sampling circuits, each connected to said digitizer through respective output switches, and said samples are sequentially applied to said digitizer with a delay by controlling said output switches.

10. (Original) A method as claimed in claim 9, wherein said activation signal is generated by comparing said input signal with a predetermined threshold.

11. (Original) A method as claimed in claim 10, wherein said sampling circuits each comprise a capacitor.

12. (Original) A method as claimed in claim 11, wherein said sampling circuits comprise eight said capacitors.

13. (Currently Amended) A pacemaker comprising:

a front end for receiving an analog input signal including a comparator for comparing said input signal with a threshold value, said front end generating an activation signal when said input signal reaches said threshold value;

a sample-and-hold circuit including storage elements for storing ~~a plurality of~~ successive groups of samples of said input signal;

a digitizer for producing a digital output signal, said digitizer being switchable, in response to said activation signal, between a power saving mode, in which said digitizer is inactive, and a reconstruction mode, in which said digitizer is operational; and

a control element for ~~controlling switches to~~ sequentially ~~apply said stored samples to said digitizer in response to said activation signal so as to output a digitized version of said input signal as it existed prior to said activation signal~~ applying incoming samples of said analog input signal in a cyclic fashion to said storage elements, said control element further, when said digitizer is in said reconstruction mode, sequentially applying samples of said analog input signal stored in said storage elements to said digitizer with a predetermined delay relative to said incoming samples so as to permit said digitizer to output a portion of said input signal that arrived at said input prior to the occurrence of said activation signal.

14. (Currently Amended) A pacemaker as claimed in claim 13, wherein said ~~sample-and-hold circuit comprises a plurality of sampling circuits~~ storage elements are connected to said digitizer through respective output switches controlled by said control element.

15. (Currently Amended) A pacemaker as claimed in claim 14, wherein said ~~plurality of sampling circuits~~ storage elements are each connected to ~~said digitizer~~ an input through respective input switches controlled by said control element.

16. (Original) A pacemaker as claimed in claim 13, further comprising a RAM for storing said digitized version of said input signal as it existed prior to said activation signal.

17. (Original) A pacemaker as claimed in claim 13, wherein said control element is a state machine.